ABSTRACT OF THE DISCLOSURE

An address translation apparatus and method that can convert a limited-range memory address from a peripheral device to an expanded-range memory address on

5   the fly. The invention can expand the limited address capability of a peripheral bus, such as a PCI bus with a 4 GB address range, to a much larger address capability, such as a 64 GB address range. This conversion can be performed on the fly by hardware, so that no appreciable delay in transfer time is created. The conversion can be performed by adding features to a conventional graphics controller interface,

10   thus minimizing the impact on circuit complexity and system cost.